AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus for randomly outputting data stored sequentially in a memory, comprising:

means for generating a first index ~~representing~~ associated with a location in said memory;

means for comparing a reference parameter representative of the size of a block of input data stored in said memory to said first index; ~~and~~

means for outputting data stored in said memory location if said ~~reference parameter~~ first index is less than or equal to said ~~first index~~ reference parameter; and

means for generating a second index if said first index is greater than said reference parameter.

2. (Cancelled)

3. (Original) The apparatus of claim 2, wherein said means for generating said first index comprises an index generator for generating said first or second index upon input of a primary or a secondary control signal, respectively.

4. (Original) The apparatus of claim 3, wherein said primary control signal is a signal periodically received by said means for generating said first index to initiate the generation of said first index.

5. (Currently Amended) The apparatus of claim 4, wherein said secondary control signal is a signal generated by said apparatus if said ~~reference parameter~~ first index is greater than said ~~first index~~ reference parameter and received by said means for generating said second index to initiate the generation of said second index.

6. (Currently Amended) The apparatus of claim 5, wherein said means for comparing comprises a comparator for receiving said index from said first index generator and said reference parameter and outputting said secondary control signal if said ~~index~~ reference parameter is less than or equal to said ~~reference parameter~~ first index.

7. (Original) The apparatus of claim 6, wherein said means for outputting data, comprises an address generator for generating a memory output command upon input of a third control signal.

8. (Original) An apparatus for randomly outputting data stored sequentially in a memory, comprising:

a delay for receiving a first control signal at a first time period, outputting a second control signal at a second time period, and outputting a third control signal at a third time period;

an index generator for receiving one of said first control signal and a fourth control signal and outputting an index upon receipt of said first or fourth control signal, said index representing a location in said memory; and

a comparator for comparing said index to a reference parameter representative of the size of said data stored in said memory, and outputting upon receipt of said second control signal to said index generator said fourth control signal if said index is greater than said reference parameter.

9. (Original) The apparatus of claim 8, wherein said third time period is greater than said second time period and less than said first time period.

10. (Original) The apparatus of claim 9, further comprising an address generator for receiving said index, and outputting to said memory a memory address represented by said index upon receipt of said third control signal.

11. (Original) The apparatus of claim 10, wherein said memory outputs data located at said memory address.

12. (Currently Amended) A method of outputting stored data from a memory, comprising the steps of:

sequentially storing input data into said memory;

determining the size of the stored input data;

receiving a first control signal and generating a first index;

comparing said first index to said data size and generating a second index if said first index is greater than said data size;

~~generating a second control signal;~~

outputting a memory address associated with said first index if said second index is not generated; and

outputting a memory address associated with said second index if said second index is generated.

13. (Original) An interleaver under control of a controller and having an address generator for outputting an address to a memory, said memory sequentially storing input data and outputting data stored at said address upon receipt of said address, said controller determining a data size of said input data, comprising:

a delay for receiving a primary index enable signal and outputting a comparator enable signal at a first time period, and outputting an address generator enable signal at a second time period;

an index generator for receiving one of said primary index enable signal and a secondary index enable signal, and outputting an index upon receipt of said primary index enable signal or said secondary index enable signal; and

a comparator for comparing upon receipt of said comparator enable signal said index and said data size and outputting said secondary index enable signal if said index is greater than said data size;

wherein an input of said address generator is connected to the output of said index generator, and outputs upon receipt of said address generator enable signal a memory address associated with a most recently generated index.

14. (New) An apparatus for randomly outputting data stored sequentially in a memory, comprising:

a delay for receiving a first control signal at a first time period, outputting a second control signal at a second time period, and outputting a third control signal at a third time period;

an index generator for receiving one of said first control signal and a fourth control signal

and outputting an index upon receipt of said first or fourth control signal, said index associated with a location in said memory; and

a comparator for comparing said index to a reference parameter representative of the size of said data stored in said memory, and outputting upon receipt of said second control signal to said index generator said fourth control signal if said reference parameter is greater than said index.

15. (New) The apparatus of claim 14, wherein said third time period is greater than said second time period and less than said first time period.

16. (New) The apparatus of claim 15, further comprising an address generator for receiving said index, and outputting to said memory a memory address represented by said index upon receipt of said third control signal.

17. (New) The apparatus of claim 16, wherein said memory outputs data located at said memory address.